What is claimed is:

1. A method of providing a switching point voltage for an integrated circuit by using a differential input buffer circuit, comprising:

determining available first and second reference voltages in the integrated circuit;

computing a switching point voltage based on the available first and second reference voltages to maximize high and low noise margins of the integrated circuit; and

setting the switching point voltage by sizing transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to a supply voltage node and the first and second reference voltages based on the computed switching point voltage.

2. The method of claim 1, further comprising:

sizing transistors in the differential input buffer to a specific speed of operation based on a load driven by the differential input buffer.

3. The method of claim 1, wherein computing the switching point voltage comprises computing the switching point voltage based on

((first reference voltage + second reference voltage)/2).

4. A method of providing a switching point voltage for an integrated circuit by using a differential input buffer circuit, comprising:

determining available first and second reference voltages in the integrated circuit using a supply voltage as the first reference voltage;

computing a switching point voltage based on the available first and second reference voltages to maximize high and low noise margins of the integrated circuit;

setting the switching point voltage by applying the supply voltage across the

gate to source voltages of transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to the supply voltage node and the first and second reference voltages based on the computed switching point voltage; and

providing the switching point voltage based on the set switching point voltage.

5. The method of claim 4, wherein coupling the input stage to the second reference voltage comprises coupling the input stage to ground.

6. The method of claim 4, wherein computing the switching point voltage comprises computing the switching point voltage based on

((first reference voltage + second reference voltage)/2).

7. A method of designing a differential input buffer circuit to provide a switching point voltage for an integrated circuit, comprising:

determining a required switching point voltage for the integrated circuit to maximize high and low noise margins of the integrated circuit;

defining required first and second reference voltages based on the determined switching point voltage; and

sizing transistors in the differential input buffer circuit including cross-coupled pairs of transistors coupled to a supply voltage node and the first and second reference voltages to provide the switching point voltage based on the defined first and second reference voltages to maximize high and low noise margins.

8. The method of claim 7, wherein determining a required switching point voltage for the integrated circuit comprises averaging the first and second reference voltages.

9. A method, comprising:

coupling a first pair of NMOS and PMOS transistors between a third pair of PMOS and NMOS transistors, respectively;

coupling a second pair of NMOS and PMOS transistors between a fourth pair of PMOS and NMOS transistors, respectively;

coupling the third pair of PMOS and NMOS transistors between a first current source node and a first current sink node;

coupling the fourth pair of PMOS and NMOS transistors between a second current source node and a second current sink node; and

coupling a fifth pair of PMOS and NMOS transistors between a third current source node and a third current sink node, wherein a gate of the fifth pair PMOS transistor is coupled to a drain of the second pair NMOS transistor and a gate of the fifth pair NMOS transistor is coupled to a drain of the first pair PMOS transistor.

10. The method of claim 9, further comprising:

coupling gates of the first pair NMOS transistor and the second pair PMOS transistor to each other and to an input terminal; and

coupling drains of the fifth pair PMOS and NMOS transistors to an output terminal.

11. The method of claim 10, further comprising:

coupling a gate of the fourth pair PMOS transistor coupled to a gate of the third pair PMOS transistor;

coupling the gates of the third and fourth PMOS transistors to drain of the first pair of NMOS transistor;

coupling gate of the fourth pair of NMOS transistor to gate of the third pair of NMOS transistor; and

coupling the gates of the third and fourth NMOS transistors to a drain of the

second pair PMOS transistor.

12. A method of forming a cross-coupled differential input buffer circuit, comprising:

forming an input stage by coupling a first pair of NMOS and PMOS transistors between a third pair of PMOS and NMOS transistors, respectively, and coupling a second pair of NMOS and PMOS transistors between a fourth pair of PMOS and NMOS transistors, respectively, and wherein coupling the third pair of PMOS and NMOS transistors between a first current source node and a first current sink node, and wherein coupling the fourth pair of PMOS and NMOS transistors between a second current source node and a second current sink node; and

forming an output stage by coupling a fifth pair of PMOS and NMOS transistors between a third current source node and a third current sink node, wherein coupling the output stage to the input stage by coupling a gate of the fifth pair PMOS transistor to the drain of the second pair NMOS transistor and further coupling a gate of the fifth pair NMOS transistor to a drain of the first pair PMOS transistor.

13. The method of claim 12, further comprising:

coupling gates of the first pair NMOS transistor and the second pair PMOS transistor to each other and to an input terminal; and

coupling drains of the fifth pair PMOS and NMOS transistors to an output terminal.

14. The method of claim 13, further comprising:

coupling gates of the first pair NMOS transistor and the second pair PMOS transistor to each other and to an input terminal; and

coupling drains of the fifth pair PMOS and NMOS transistors to an output terminal.

15. The method of claim 14, further comprising:

coupling a gate of the fourth pair PMOS transistor to a gate of the third pair PMOS transistor;

coupling the gates of the third and fourth PMOS transistors to drain of the first pair of NMOS transistor;

coupling gate of the fourth pair of NMOS transistor to gate of the third pair of NMOS transistor; and

coupling the gates of the third and fourth NMOS transistors to a drain of the second pair PMOS transistor.

16. A method of forming an integrated circuit, comprising:

coupling a first pair of NMOS and PMOS transistors between a current source node and a first current sink node, wherein a drain of the first pair NMOS transistor is coupled the first current source node and a drain of the first pair PMOS transistor is coupled to the first current sink node, and wherein a source of the first pair NMOS transistor is coupled to a source of the first pair PMOS transistor;

coupling a second pair of NMOS and PMOS transistors between a second current source node and a second current sink node, wherein a drain of the second pair NMOS transistor is coupled to the second current source node and a drain of the second pair PMOS transistor is coupled to the second current sink node, wherein a source of the second pair NMOS transistor is coupled to a source of the second pair PMOS transistor, and wherein gates of the first pair of NMOS transistor and the second pair PMOS transistor are coupled to each other and to an input terminal to receive a supply voltage;

coupling a third pair of PMOS and NMOS transistors between the first current source node and the first current sink node, wherein a source of the third pair PMOS transistor is coupled to the first current source node, and wherein a drain of the third pair PMOS transistor is coupled to a drain of the first pair NMOS transistor, wherein a drain of the third pair NMOS transistor is coupled to drain of

the first pair PMOS transistor, and wherein a source of the third pair NMOS transistor is coupled to the first current sink node;

coupling a fourth pair of PMOS and NMOS transistors between the second current source node and the second current sink node, wherein a source of the fourth pair of PMOS transistor is coupled to the second current source node, wherein a drain of the fourth PMOS transistor is coupled to the drain of the second pair NMOS transistor, wherein a drain of the fourth NMOS transistor is coupled to the drain of the second pair PMOS transistor, and wherein a source of the fourth NMOS transistor is coupled to the second current sink node; and

coupling a fifth pair of PMOS and NMOS transistors between a third current source node and a third current sink node, wherein a source of the fifth pair PMOS transistor is coupled to the third current source node, wherein a gate of the fifth pair PMOS transistor is coupled to the drain of the second pair NMOS transistor and further coupled to a drain of the fourth pair PMOS transistor, and wherein a drain of the fifth pair PMOS transistor and a drain of the fifth pair NMOS transistor and further the drains of the fifth pair NMOS and PMOS transistors are coupled to an output terminal.

17. The method of claim 16, further comprising:

coupling a gate of the fourth pair PMOS transistor to the gate of the third pair PMOS transistor; and

coupling gates of the third and fourth pair PMOS transistors to the drain of the first pair NMOS transistor.

18. The method of claim 17, further comprising:

coupling a gate of the fourth pair NMOS transistor to a gate of the third pair NMOS transistor; and

coupling gates of the third and fourth pair NMOS transistors to a drain of the second pair PMOS transistor and drain of the fourth pair of NMOS transistor.

19. The method of claim 18, further comprising:

coupling a gate of the first pair PMOS transistor to a second source voltage; and

coupling a gate of the second pair NMOS transistor to a first source voltage.

20. A method of forming an input buffer circuit, comprising:

coupling a first pair of NMOS and PMOS transistors between a first current source node and a first current sink node such that a drain of the first pair NMOS transistor is coupled to the first current source node and a drain of the first pair PMOS transistor is coupled to the first current sink node, and further a source of the first pair NMOS transistor is coupled to a source of the first pair PMOS transistor;

coupling a second pair of NMOS and PMOS transistors between a second current source node and a second current sink node such that a drain of the second pair NMOS transistor is coupled to the second current source node and a drain of the second pair PMOS transistor is coupled to the second current sink node, and further a source of the second pair NMOS transistor is coupled to a source of the second pair PMOS transistor, and wherein gates of the first pair of NMOS transistor and the second pair PMOS transistor are coupled to each other and to an input terminal to receive a supply voltage;

coupling a third pair of PMOS and NMOS transistors between the first current source node and the first current sink node such that a source of the third pair PMOS transistor is coupled to the first current source node, and a drain of the third pair PMOS transistor is coupled to the drain of the first pair NMOS transistor, and further a drain of the third pair NMOS transistor is coupled to the drain of the first pair PMOS transistor, and wherein a source of the third pair NMOS transistor is coupled to the first current sink node;

coupling a fourth pair of PMOS and NMOS transistors between the second current source node and the second current sink node such that a source of the

fourth pair of PMOS transistor is coupled to the second current source node, and a drain of the fourth PMOS transistor is coupled to the drain of the second pair NMOS transistor, and further a drain of the fourth pair NMOS transistor is coupled to the drain of the second pair PMOS transistor, and wherein a source of the fourth NMOS transistor is coupled to the second current sink node; and

coupling a fifth pair of PMOS and NMOS transistors between a third current source node and a third current sink node such that a source of the fifth pair PMOS transistor is coupled to the third current source node, and a gate of the fifth pair PMOS transistor is coupled to the drain of the second pair NMOS transistor, and further coupled to a drain of the fourth pair PMOS transistor, and wherein a drain of the fifth pair PMOS transistor and a drain of the fifth pair NMOS transistor and further the drains of the fifth pair NMOS and PMOS transistors are coupled to an output terminal.

21. The method of claim 20, further comprising:

coupling a gate of the fourth pair PMOS transistor to a gate of the third pair PMOS transistor; and

coupling gates of the third and fourth pair PMOS transistors to the drain of the first pair NMOS transistor.

22. The method of claim 21, further comprising:

coupling a gate of the fourth pair NMOS transistor to a gate of the third pair NMOS transistor; and

coupling gates of the third and fourth pair NMOS transistors to the drain of the second pair PMOS transistor and drain of the fourth pair of NMOS transistor.

23. The method of claim 22, further comprising:

coupling a gate of the first pair PMOS transistor to a second reference voltage; and

coupling a gate of the second pair NMOS transistor to a first reference voltage.

24. A method of forming a semiconductor circuit, comprising:

coupling a first pair of NMOS and PMOS transistors between a first current source node and a first current sink node such that a drain of the first pair NMOS transistor is coupled to the first current source node and a drain of the first pair PMOS transistor is coupled to the first current sink node, and further a source of the first pair NMOS transistor is coupled to a source of the first pair PMOS transistor;

coupling a second pair of NMOS and PMOS transistors between a second current source node and a second current sink node such that a drain of the second pair NMOS transistor is coupled to the second current source node and a drain of the second pair PMOS transistor is coupled to the second current sink node, and further a source of the second pair NMOS transistor is coupled to a source of the second pair PMOS transistor, wherein the gates of the first pair of NMOS transistor and the second pair PMOS transistor are coupled to each other and to an input terminal to receive a supply voltage, wherein a gate of the first pair PMOS transistor is coupled to a second reference voltage, and wherein a gate of the second pair NMOS transistor is coupled to a first reference voltage;

coupling a third pair of PMOS and NMOS transistors between the first current source node and the first current sink node such that a source of the third pair PMOS transistor is coupled to the first current source node, and a drain of the third pair PMOS transistor is coupled to the drain of the first pair NMOS transistor, and further a drain of the third pair NMOS transistor is coupled to the drain of the first pair PMOS transistor, and wherein a source of the third pair NMOS transistor is coupled to the first current sink node;

coupling a fourth pair of PMOS and NMOS transistors between the second current source node and the second current sink node such that a source of the

fourth pair of PMOS transistor is coupled to the second current source node, and a drain of the fourth PMOS transistor is coupled to the drain of the second pair NMOS transistor, and further a drain of the fourth pair NMOS transistor is couple to the drain of the second pair PMOS transistor, wherein a source of the fourth pair NMOS transistor is coupled to the second current sink node, wherein a gate of the fourth pair PMOS transistor is coupled to the gate of the third pair PMOS transistor, and gates of the third and fourth pair PMOS transistors are coupled to the drain of the first pair NMOS transistor, wherein a gate of the fourth pair NMOS transistor is coupled to a gate of the third pair NMOS transistor, and wherein gates of the third and fourth pair NMOS transistors are coupled to the drain of the second pair PMOS transistor and drain of the fourth pair of NMOS transistor; and

coupling a fifth pair of PMOS and NMOS transistors between a third current source node and a third current sink node such that a source of the fifth pair PMOS transistor is coupled to the third current source node, and a gate of the fifth pair PMOS transistor is coupled to the drain of the second pair NMOS transistor, and further coupled to a drain of the fourth pair PMOS transistor, and wherein a drain of the fifth pair PMOS transistor, a drain of the fifth pair NMOS transistor, and the drains of the fifth pair NMOS and PMOS transistors are coupled to an output terminal.